REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 2, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-21 are under consideration in this application. Claims 1, 3-11, 15-16 and 18-20 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. A new claim 21 is being added to recite another embodiment described in the specification.

Additional Amendments

The specification and the claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejections

The current title of the invention was objected to being too broad. Claim 8 was objected under 37 CFR 1.75(c) on the grounds that it is in an improper form, and thus claim was not examined. Claims 1, 5, 8-11, 15 and 16 were objected to informalities. Claims 11-16 were rejected under 35 U.S.C. § 112, second paragraph due to their g of essential structural connectors. As indicated, the specification and the claims have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Allowed Subject Matters

Claims 9 and 10 were allowed for reciting a self-construction circuit.

Prior Art Rejections

Claims 1-7, 11-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Pat. No. 6,233,182 to Satou et al. (hereinafter "Satou"). The prior art references of Vincent et al (4,633,392), Yoshizawa et al. (5,749,089), Chesley (4,333,142), Morrill, Jr. et al (4,129,903), Hiraki et al (6,201,733), Satou et al. (6,467,056), Ho et al. (6,009,251), Sample et al. (5,841,967), and Joly et al. (6,178,541) were cited as being pertinent to the present application. This rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit according to the invention, as now recited in claim 11, has at least one self-construction circuit comprising: storing means for storing information obtained from a description in which a newly assigned logical function is represented in a hardware description language (HDL) and for obtaining an output according to the newly assigned logical function with respect to an input signal supplied to an address terminal thereof; and means for verifying a correlation between the output signal and the input signal complying with the newly assigned logical function ("*self-verification*" of the self-construction circuit page 6, line 20).

In particular, the self-construction circuit 10 (Fig. 2; page 5, lines 2-12), as now recited in claim 1, comprising: storing means 11 for reading data therefrom and writing data thereinto; comparing means 20 (Fig. 4) for providing a comparison result; and variable address converting means 30 (Fig. 3) for converting an address signal ***In*** inputted to said self-construction circuit 10 into a write address in the storing means 11 ("*previously stored address*" page 16, line 6) for writing into the storing means 11 input data of a hardware description language (HDL) statement of a newly designated logical function ("*writes the data input from the external to the memory cell via the input/output & comparator* "page 16, lines 11-12) based on the comparison result ***CM*** by the comparing means 20. The comparing means 20 compare input data continuously supplied to said self-construction circuit with the input data written into and then read from the storing mean 11 ("*compares the data read from the memory array 11 with the write data input to the data input/output terminal 42...to generate a comparison result signal signal* ***CM***" page 16, lines 19-21). The input data is written to the storing means 11 so that data read from the storing means 11 is an expected output signal according to the newly designated logical function with respect to an input signal of the self-construction circuit. The"*self-verification*" of the self-construction circuit is executed via match or mismatch of ***CM*** and the internal incriminator (page 16, last paragraph to page 17, second paragraph).

In addition to **being constructed to operate a desired logical function** ("*constructs a logic circuit having a desired logical function in accordance the HDL descriptive statement using the self-construction circuit of the first embodiment" page 18, last paragraph*), the self-construction circuit according to the invention also **self-tests the memory array therein**. "*When both data match, the write control circuit 34 outputs a write end signal WF to the external and the data write operation for one address terminates (step S16). When an external control circuit receives the write end signal WF, the next address signal is generated and input to the address input terminal 41.... If an error is detected in the decision, an address is updated and the data is written to the next address position. Accordingly, even if there is a defect in the memory array 11, the address is automatically skipped and the data is written to the next address. Thus, in the self-construction circuit of this embodiment, there is an advantage that all the memory cells of the memory array 11 need not to be normal, and previous test whether there is a detective bit in the memory array 11 is not needs* (page 17, 2nd paragraph to page 18, 1st paragraph)."

The invention is also directed to a method for constructing a logic integrated circuit (Fig. 5), as now recited in claim 8, comprising: providing at least one self-construction circuit capable of being converted to operating different logical functions as a building block for the logic integrated circuit; assigning a desired logical function to said self-construction circuit by sending an address signal to the self-construction circuit; self-decoding design data coded at logical function level of the desired logical function by the self-construction circuit; self-converting by the ***self-construction*** circuit to operate according to the desired logical function; and ***self-verifying*** operation by the self-construction circuit with the desired logical function. An example is provided from page 19 third paragraph.

Applicants respectfully contend that neither Satou nor any other cited reference teaches or suggests such a self-construction circuit or self-construction/verification method according to the invention. As admitted by the Examiner (page 8, paragraph no. 26 of the outstanding Office Action), claims 9 and 10 were allowed for reciting the self-construction circuit. Accordingly, the independent claims 1, 8 and 11 as well as their dependent claims claimed are now inguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate

the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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